Claims

What is claimed is:

1. A method for controlling curvature of a power transistor device comprising a device film formed on a substrate, the method comprising the steps of:

thinning the substrate, the device having an overall residual stress attributable at least in part to the thinning step; and

applying a stress compensation layer to a surface of the device film, the stress compensation layer having a tensile stress sufficient to counterbalance at least a portion of the overall residual stress of the device.

2. The method of claim 1, wherein the stress compensation layer comprises a thin film.

3. The method of claim 1, wherein the power transistor comprises a DMOS device.

4. The method of claim 1, wherein the device substrate is thinned using aggressive backside substrate removal processing.

5. The method of claim 2, wherein the thin film comprises a dielectric material comprising at least one of a silicon nitride, a silicon oxide, a silicon oxynitride, an oxynitride, a nitride and combinations comprising at least one of the foregoing dielectric materials.

6. The method of claim 2, wherein the thin film is applied using a deposition technique comprising at least one of sputtering, chemical vapor deposition, electroplating and spin-on processing.

7. The method of claim 1, wherein the steps of thinning and applying are performed repeatedly until a desired curvature is attained.

8. The method of claim 2, wherein the thin film serves as an encapsulating layer.

9. The method of claim 1, wherein the stress compensation layer applied to the surface of the device changes the curvature of the device.

10. The method of claim 1, wherein the stress compensation layer applied to the surface of the device maintains the curvature of the device.

11. The method of claim 1, further comprising the step of monitoring the curvature of the device.

12. The method of claim 11, wherein the curvature of the device is monitored using an off-axis optical laser technique.

13. A power transistor device comprising:

a substrate; and

a device film formed on the substrate, the device having an overall residual stress attributable at least in part to a thinning process applied to the substrate;

wherein the power transistor device further comprises a stress compensation layer formed on a surface of the device film, the stress compensation layer having a tensile stress that counterbalances at least a portion of the overall residual stress of the device.

14. The device of claim 13, wherein the stress compensation layer comprises a thin film.

15. The device of claim 14, wherein the thin film comprises an encapsulating layer.

16. An integrated circuit, comprising:

at least one power transistor device comprising a substrate and a device film formed on the substrate, the device having an overall residual stress attributable at least in part to a thinning process applied to the substrate;

wherein the power transistor device further comprises a stress compensation layer formed on a surface of the device film, the stress compensation layer having a tensile stress that counterbalances at least a portion of the overall residual stress of the device.